UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,856	08/29/2003	Bernd Goller	MAS-FIN-403	9446

24131 7590 10/06/2005

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/651,856	GOLLER ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/25/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29 and 31-41* is/are pending in the application.

4a) Of the above claim(s) *1-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-29 and 31-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 25, 2005 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24-29 and 31-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US 6515355), hereinafter Jiang in view of Takeuchi et al. (US 6548598), hereinafter Takeuchi.

Regarding claim 24, Fig. 9A of Jiang shows an electronic component with a semiconductor chip, comprising:

a multilayer plastic embedding compound [12', 24', 56] embedding the semiconductor chip [20'], said multilayer compound forming a first plastic layer [56] and a second plastic layer [12'; a plastic substrate]

the semiconductor chip having an active surface and a passive surface, the passive surface being embedded in said first plastic layer;

the semiconductor chip having marginal sides surrounded, up to a partial height thereof, by said first plastic layer;

said first plastic layer surrounding the semiconductor chip;

said first plastic layer having an upper boundary adjoining said second plastic layer located thereabove;

said second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

said second plastic layer having a level upper side forming a boundary interface to at least one further component plane; and

at least one wiring structure [22' or conductive trace] disposed above said second plastic layer, said wiring structure having through-contacts [54] between contact regions of the semiconductor chip and external contacts of the electronic component [through a solder ball 14'].

Fig. 9A of Jiang shows substantially the entire claimed structure except "said first plastic layer having a bead." Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Takeuchi into the device of Jiang in order to have the first plastic layer filled with glass beads to form a denser plastic layer.

Regarding claim 25, it is intrinsic that Fig. 9A of Jiang shows said first plastic layer is formed with a plastic embedding compound having different levels of crosslinking staggered vertically, with a highest level of crosslinking being arranged in a region of a base surface of said first plastic layer since the first plastic layer is treated to form a crosslinked siloxane network

[col. 3, line 60- col. 4, line 4]. In addition, note that "crosslinking staggered vertically and crosslinking being arranged" are a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 26, it is intrinsic that Fig. 9A of Jiang shows said first plastic layer is formed with a plastic embedding compound having a completely crosslinked region at a base plate and a precrosslinked region thereabove through forming a crosslinked siloxane as discussed in claim 25.

Regarding claims 27 and 28, Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46], therefore, the spherical particles forming spacers for the semiconductor chips in the first plastic layer and having a uniform predefined diameter through being a glass bead.

Regarding claim 29, Jiang discloses that said second plastic layer has a polyimide resin forming a leveling compensating compound [col. 2, lines 54-55]. Also, note that "forming a leveling compensating compound" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 31, Fig. 9A of Jiang shows an electronic component with an electronic component with a semiconductor chip, comprising:

a multilayer plastic embedding compound [12', 56, 24'] embedding the semiconductor chip [20'], said multilayer compound forming a first plastic layer [12'] and a second plastic layer [56];

the semiconductor chip having an active surface and a passive surface, the active surface being embedded in said first plastic layer [12'];

the semiconductor chip having marginal sides surrounded, up to a partial height thereof, by said first plastic layer;

said first plastic layer having an upper boundary adjoining said second plastic layer located thereabove;

said second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

said second plastic layer having a level upper side forming a boundary interface to at least one further component plane; and

at least one wiring structure [conductive trace; col. 3, lines 9-11] disposed above said first plastic layer, said wiring structure having through-contacts [54] between contact regions of the semiconductor chip and external contacts of the electronic component [through the electrodes 14'].

Fig. 9A of Jiang shows substantially the entire claimed structure except "said first plastic layer having a bead." Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Takeuchi into the device of Jiang in order to have the first plastic layer filled with glass beads to form a denser plastic layer.

Regarding claim 32, Fig. 9A of Jiang shows the active surface of the semiconductor chip [20'] projects from said first plastic layer [12'].

Regarding claim 33, Fig. 9A of Jiang shows a portion of a blank with a plurality of component positions for electronic components, each having at least one semiconductor chip, the blank comprising:

a first plastic layer [56] surrounding the semiconductor chips on marginal sides and up to a partial height thereof;

a second plastic layer [12'] above said first plastic layer, said first plastic layer having an upper boundary to said second plastic layer;

the semiconductor chip having an active surface and a passive surface, the passive surface being embedded in said first plastic layer;

said first plastic layer surrounding the semiconductor chip

said second plastic layer resting on regions of the marginal sides of the semiconductor chips not covered by said first plastic layer;

a further component plane defined above said second plastic layer, and said second plastic layer having a level upper side forming an interface to said further component plane [through a solder ball 14'];

wiring structures [conductive trace; col. 3, lines 9-11] with through-contacts [54] between contact regions of the semiconductor chips and external contacts of electronic components disposed above at least one of said second plastic layer and the semiconductor chips;

at least one of said first and second plastic layers being at least partly cured [col. 3, line 24 – col. 4, line 40] and forming a self-supporting, substantially dimensionally stable, multilayer plastic plate.

Fig. 9A of Jiang shows substantially the entire claimed structure except "said first plastic layer having a bead." Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Takeuchi into the device of Jiang in order to have the first plastic layer filled with glass beads to form a denser plastic layer.

The subject matters regarding claims 34 and 35 have been discussed in claims 25 and 26 concurrently.

The subject matters regarding claims 36-38 have been discussed in claims 27-29 concurrently.

Regarding claim 39, Fig. 9A of Jiang shows said wiring structure is covered by adhesive material [24; epoxy] on interfaces to a plastic plate formed by said first and second layers.

Regarding claim 40, Fig. 9A of Jiang shows a portion of a blank which forms a plurality of component positions for electronic components, each having at least one semiconductor chip [18], the blank comprising:

a first plastic layer [56] surrounding the semiconductor chips on marginal sides and up to a partial height thereof;

a second plastic layer [12'] above said first plastic layer, said first plastic layer having an upper boundary to said second plastic layer;

the semiconductor chip having an active surface and a passive surface, the passive surface being embedded in said first plastic layer;

the semiconductor chip having marginal sides surrounded, up to a partial height thereof, by said first plastic layer;

said first plastic layer surrounding the semiconductor chip;

said first plastic layer having a upper boundary adjoining said second plastic layer located thereabove;

said second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

a further component plane defined above said second plastic layer, and above said second plastic layer having a level upper side forming an interface to said further component plane; wiring structures [22' or conductive trace] with through-contacts [54] between contact regions of the semiconductor chips and external contacts of the electronic component [through a solder ball 14'] disposed at least one of second plastic layer and semiconductor chips [Fig. 7].

at least one of said first and second plastic layers being at least partly cured [col. 3, line 24 – col. 4, line 40] and forming a self-supporting, substantially dimensionally stable, multilayer plastic plate.

Fig. 9A of Jiang shows substantially the entire claimed structure except "said first plastic layer having a bead." Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Takeuchi into the device of Jiang in order to have the first plastic layer filled with glass beads to form a denser plastic layer.

Regarding claim 41, Fig. 9A of Jiang shows the active surface of the semiconductor chip [20'] projects from said first plastic layer [56].

Response to Arguments

Applicant's arguments filed July 25, 2005 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant. New rejections are made in response to Applicant amended claims. And below are the Examiner's remarks in response to Applicant's argument.

Applicant mainly argues that "an FR4 board and siloxane are plastic, a person skilled in the art would not consider them as 'plastic embedding compound' ." Note that pending claim recites a limitation "a multilayer plastic embedding compound embedding the semiconductor chip, said multilayer compound forming a first plastic layer and a second plastic layer." Fig. 9A of Jiang reads on this limitation. In detail, Fig. 9A of Jiang shows that a multilayer plastic embedding compound [12', 24', 56] which embeds a semiconductor chip and said multilayer compound forms a first plastic layer [56] and a second plastic layer [12']. It is pointed out that Jiang et al. explicitly discloses that a semiconductor chip is embedded partially in a PPMS layer [56] and a plastic substrate [12']. It is also pointed out that a multilayer plastic embedding compound in the instant invention is two layered and each of the two layer is formed of different material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

Steven Loke